RF System Concepts for Highly Integrated RFICs for W-CDMA Mobile Radio Terminals

Andreas Springer, *Member, IEEE*, Linus Maurer, and Robert Weigel, *Senior Member, IEEE*

Invited Paper

***Abstract*—The standardization phase for third-generation wide-band CDMA systems like the universal mobile telecommunication system, which will add broad-band data to support video, Internet access, and other high-speed services for untethered devices is running toward its finalization. As is typical for mobile communication systems standardization, sufficient RF performance has been assumed and most efforts have been put to digital baseband issues. This is especially true for the mobile phone transceivers, the RF part of which is (although its baseband part is much more complex in terms of number of devices) still the bottleneck of the entire system. Meanwhile, in the RF concept engineering of today's commercial products, an accurate prediction of the needed RF performance by using RF system simulation is indispensable. This is, in particular, the case with third-generation wireless systems, which, from the RF design point-of-view, are quite different from second-generation time-division multiple access/frequency-division multiple-access systems due to the fact that the user signals are now separated in the code domain rather than in the time and/or frequency domain. The paper gives an insight of how to derive receiver requirements for third-generation mobiles in terms recognizable by microwave designers, reports on the system simulation-based design, and performance of silicon-based RF integrated circuits for mobile terminal use, and discusses some future technologies and techniques and their possible impact on portable wireless devices.**

***Index Terms*—CDMA, radio communication, receiver architectures, RFIC, spread-sprectrum communication, UMTS.**

I. Introduction

THE RF integrated circuit (RFIC) market has expanded greatly during the last few years. Wireless devices such as cellular and cordless phones, pagers, global positioning system (GPS) devices, and RF identification tags are especially rapidly penetrating all aspects of our daily lives. Two sources for this remarkable establishment of the RFIC market can be identified. First of all, the development of low-cost production facilities for the mass production of highly integrated silicon-based circuits with bipolar transistors capable of operating at gigahertz frequencies, which appeared about ten years ago. A second reason for the establishment of the RFIC market came up about the same time with the introduction of the global system for mobile communications (GSM) in Europe [1]. Since the telecommunication authorities of the European countries agreed to implement this standard, a big market was created, which required high-quality and low-cost chip sets. In the following years, both market and technology developed rapidly because of this fruitful technology-push/market-pull situation. It is expected that the advent of third-generation (3G) mobile communication systems, summarized as international mobile telecommunication systems (IMT-2000), as well as other wireless applications like, e.g., Bluetooth [2], wireless local area networks (WLANs) [3], wireless local loop (WLL) [4], etc., will further support the development of the RFIC market.

Besides supplying the required functionality, any successful RFIC solution has to be cheap, small, and must run at low power. The main key to attain these features is the choice of a suitable system architecture since it determines to a high degree the level of integration and the power consumption. Due to the ever-increasing integration level of RFICs, the design process also has to improve. Traditionally, for each building block (e.g., low-noise amplifier (LNA), mixer, filter, etc.), certain target specifications have been derived from the communication system demands and, subsequently, each RF building block has been independently optimized to meet these system specifications with sufficient reserve. This modular design flow has started to change into a more integral design approach. Only by considering the entire communications system including both RF and baseband functionalities, an optimum design solution is possible. This requires the involvement and understanding of baseband signal-processing techniques (e.g., coding, RAKE receiver, etc.), integrated circuit (IC) technologies, mixed-signal design issues, layout techniques, analog (RF and baseband) and digital circuit design, etc., and, therefore, RFIC design, has become a highly multidisciplinary task. In particular, the interdependency between RF and baseband signal processing will become more critical due to the steadily increasing computational power of the digital circuitry.

This paper is organized as follows. We first give an introduction into the transition scenario from second-generation (2G) to 3G cellular systems. The following section introduces some basics of the spread-spectrum technique, which is used in most of the 3G systems. A more detailed description of the UMTS frequency division duplex (FDD) mode is given in Section IV, together with some examples as to how to derive first target specifications for the receiver circuit design from system-level con-

Manuscript received May 1, 2001. This work was supported in part by the European Commission under Contract IST-1999-11081 (LEMON).

The authors are with the Institute for Communications and Information Engineering, Johannes Kepler University Linz, Linz A-4040, Austria (e-mail: r.weigel@ieee.org).

Publisher Item Identifier S 0018-9480(02)00838-4.

siderations. In Section V, based on the considerations from the preceding section, different receiver architectures are reviewed with respect to their suitability to UMTS. Then, recent UMTS receiver designs are presented, and finally, possible future trends in transceiver front-end design for 3G systems are discussed.

II. Evolution From 2G to 3G Systems

In 1985, the International Telecommunications Union (ITU) began work on 3G systems denoted as future public land mobile telephone systems (FPLMTS), which was later renamed to IMT-2000 [5]. The key factors and main objectives for 3G systems include worldwide coverage and roaming incorporating a satellite component, capacity and capability to serve more than 50% of the population [6], multimedia service capability, high-speed access, low-cost operation, and integration of residential, office, and cellular services into a single system based on one mobile terminal, which is termed user equipment (UE) in 3G terminology. Further issues are packet access [7] and an evolutionary transition from 2G to 3G. From these requirements, the fundamental demands for data throughput over the air interface were identified as 144 kb/s (preferably 384 kb/s) with full coverage and high mobility of the UE, and as up to 2 Mb/s for low mobility and coverage limited to high traffic areas [5].

Upon a request from the ITU for radio transmission technology (RTT) proposals, different regional standardization bodies submitted their proposals for IMT-2000 in 1998 [8]. Details of these proposals are available on the ITU web page.[1] The majority of the submitted proposals were based on wide-band CDMA (W-CDMA) or at least contained a W-CDMA component. During the evaluation of the different proposals by the ITU, it turned out that the vision of a global standard with a single radio interface was not realizable for 3G systems. This was due to the various 2G technologies used in different regions in the world. It would have been impossible to find one technology as an evolutionary path for all existing 2G systems. Therefore, a five-member family concept was adopted and agreed upon at the end of 1999 [9]. The five standards included in IMT-2000 are shown in Fig. 1. As so-called IMT-direct spread (IMT-DS) the UMTS terrestrial radio access FDD (UTRA FDD mode) was adopted in Europe and Japan; IMT-time-code (IMT-TC) is a combination of the UTRA time division duplex (UTRA TDD) (Europe and Japan) and the time-division synchronous CDMA (TD-SCDMA) (China) proposals; cdma2000 (U.S.) is found as IMT-muticarrier (IMT-MC); IMT-single carrier (IMT-SC) corresponds to universal wireless communications-136 (UWC-136) (U.S.), and IMT-frequency time (IMT-FT) is the European digital European cordless telephone (DECT) proposal. These five standards are now being further developed in the regional standardization bodies. For the W-CDMA-based technologies (IMT-DS and IMT-TC), the third-generation Partnership Project (3GPP) was created.[2] A similar group was established for the development of the cdma2000-based systems, called 3GPP2.[3] The 3GPP and 3GPP2 activities are coordinated and run in parallel [10].

[1][Online]. Available: http://www.itu.int/imt/2_rad_devt/proposals/index.html

[2][Online]. Available: http://www.3gpp.org

[3][Online]. Available: http://www.3gpp2.org

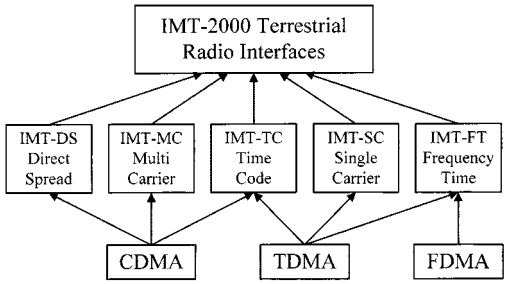

Fig. 1. Set of IMT-2000 terrestrial radio interfaces.

III. Spread-Spectrum Fundamentals

The basics of spread-spectrum (SS) technology can be derived from Shannon's well-known channel capacity formula [11]

$$C = W \log_2 \left(1 + \frac{S}{N}\right) \tag{1}$$

where C is the capacity of an additive white Gaussian noise (AWGN) channel in bits/hertz, W is the bandwidth, N is the noise power, and S is the signal power. As can be seen from (1), a low S/N can be compensated for by means of an increased transmission bandwidth. The following two criteria define an SS system [12]: the transmitted bandwidth is much higher than the bandwidth of the information signal being sent and the spreading signal is independent of the information bearing signal. An important reason for using SS is the linear dependency of the channel capacity C on the bandwidth W [see (1)], whereas C increases only with the logarithm of the signal-to-noise ratio (SNR) S/N. SS techniques have an inherent resistance against interference and jamming, which is illustrated in Fig. 2 for a direct-sequence spread spectrum (DS-SS) system. Suppose that a narrow-band interferer is present in the received signal. The despreading in the receiver recovers the original spectrum of the data signal, which has a high spectral power density and a small bandwidth. At the same time, the interference signal is spread over a much larger bandwidth and, therefore, the interference power within the receiver bandwidth decreases. To effectively obtain this increase of the wanted signal level, the locally generated code in the receiver, which is the same as is used in the transmitter, has to be exactly synchronized to the incoming wanted signal.

The best known advantages of DS-SS systems for cellular system design include the possibility of selective addressing (CDMA [13]) and the ability to eliminate the effect of multipath propagation by using RAKE receiver techniques [14] in the mobile station. Drawbacks incorporate the relatively complex structure of the RAKE receiver, a high synchronization effort, and the need of an accurate output power control in order to deal with the near–far problem [15]. The wide-band nature of the signal also leads to the necessity of wide-band modems and wide-band baseband amplifier stages. Furthermore, fast and accurate automatic gain control (AGC) circuitry is a prerequisite for an efficient handling of the multipath phenomena [12].

Neglecting imperfections and implementation details, the basic functionality and performance of SS systems can be described by a few equations. Important terms in the context

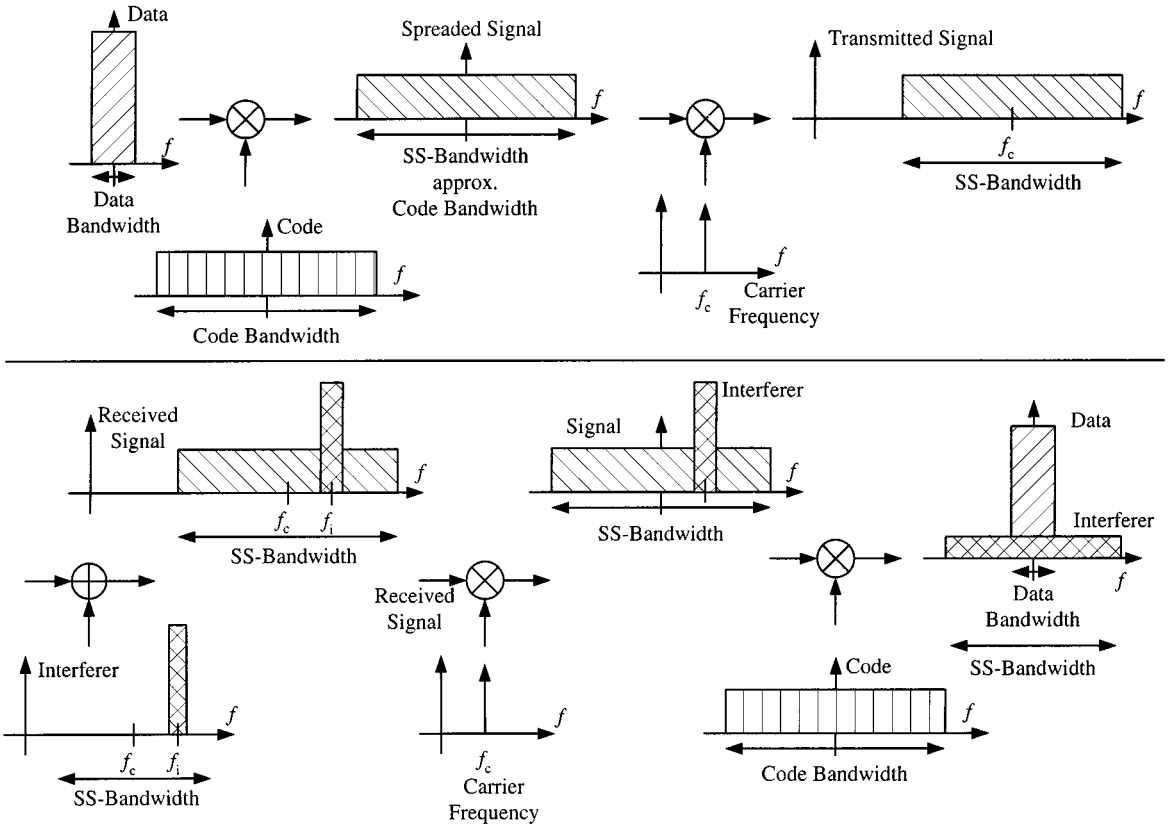

Fig. 2. Suppression of a narrow-band interferer in a DS-SS system.

of SS are the so-called spreading factor (SF) and the spreading gain (SG). SF describes the ratio of the information data rate (represented by the bit duration $T_{\rm bit}$) to the rate of the spreading code (represented by the chip duration $T_{\rm chip}$). This ratio ranges from 4 to 512 in 3GPP systems as follows:

$$\mathrm{SF} = \frac{T_{\rm bit}}{T_{\rm chip}} \tag{2}$$

$$\mathrm{SG\ [dB]} = 10 \log \mathrm{SF}. \tag{3}$$

Let us denote the chip energy to interference power spectral density (PSD) ratio $E_{\rm c}/I$ and the bit energy to interference PSD ratio $E_{\rm b}/I$. $E_{\rm c}/I$ and $E_{\rm b}/I$ appear before and after despreading in the receiver, respectively. $E_{\rm c}/I$, $E_{\rm b}/I$, and SG are then related by

$$\frac{E_{\rm b}}{I} = \frac{E_{\rm c}}{I} + \mathrm{SG} + \mathrm{OF} \tag{4}$$

where the orthogonality factor (OF) describes the degree of orthogonality between the wanted user signal and the interference signal. For example, in the case of Gaussian noise, OF equals 0 dB. Therefore, in a Gaussian noise environment, the wanted user signal level is increased by an amount of SG decibels. If only interference from other users is considered, OF approaches infinity for perfectly orthogonal signals. Thus, the choice of codes employed for the spreading of the user signals greatly influences the overall performance of a CDMA system.

These considerations are only valid for perfect synchronization of the received signal and the locally generated code used for despreading. It can be shown that a timing error of, e.g., one-half of the chip duration $T_{\rm chip}$ results in an SNR loss of 6 dB. Therefore, obtaining initial synchronization and keeping the code synchronized by a code tracking loop can be considered as key problems in SS system design [12].

IV. Receiver Requirements and 3GPP Front-End Test Cases

In what follows, we will briefly discuss four 3GPP front-end test cases. By way of these examples, it is demonstrated how RF key parameters can be derived from the 3GPP specifications. The complete set of the RF specific test cases for the 3GPP FDD mode can be found in [16], and are further discussed in [17]. In Table I, common terms from the 3GPP specifications used in the following section are described. Unless otherwise stated, all parameters are specified at the antenna connector of the UE. They are defined using the 12.2-kb/s down link (DL) reference measurement channel [16]. The total received PSD $\hat{I}_{\rm or}$ for all test cases described in the following is composed of the actual data carrying signal (DPCH) to be detected and so-called common downlink channels (pilot channel, synchronization channel, etc.), necessary for establishing and maintaining a link between the base station and UE. Therefore, $\mathrm{DPCH\_E_C}$ is usually several decibels below $\hat{I}_{\rm or}$.

A. Reference Sensitivity Level Test Case

In 3GPP, the reference sensitivity is the minimum receiver input power measured at the antenna port at which the bit error rate (BER) does not exceed a value of 10^{-3}. This test case determines the tolerable noise figure (NF) of the receiver

TABLE I
COMMON 3GPP PARAMETERS

DPCH_E_C	Average energy per chip of a dedicated physical channel (DPCH)
$\hat{I}_{or}$	Received (DL) power spectral density measured at the UE antenna connector
I_{or}	Total DL transmit power spectral density at the base station antenna connector
I_{oac}	Power spectral density of the adjacent channel measured at the UE antenna connector
I_{ouw}	Unwanted signal power level
OCNS	Orthogonal Channel Noise Simulator, a mechanism used to simulate users or control signals on the other orthogonal channels of a DL

front-end. $\hat{I}_{or}$ and DPCH_E_C are -106.7 dBm/3.84 MHz and -117 dBm/13.84 MHz, respectively. The 12.2-kb/s reference measurement channel used for this test case has a symbol rate of 30 ks/s and an SF of 128, i.e., an SG of approximately 21 dB. Let us assume that the required bit energy to interference PSD ratio $E_{b,\,req}/I$ is 5 dB [18], that the insertion loss (IL) for the baseband implementation is 2 dB, and that the coding gain (CG) is 4 dB (CG estimation is difficult for the used convolutional coder; 4 dB seems to be rather conservative). The acceptable interference signal level after despreading (P_I) then results in

$$P_I = \text{DPCH\_E}_C + \text{SG} + \text{CG} - \frac{E_{b,\,req}}{I} - \text{IL}. \quad (5)$$

Inserting the above given values, we have $P_I = -99$ dBm. This leaves a margin for the front-end NF of

$$\text{NF} = P_I - 10\log(kTB) = -99\ \text{dBm} + 108\ \text{dBm} = 9\ \text{dB} \quad (6)$$

with the Boltzmann constant k, the ambient temperature $T = 300$ K, and the bandwidth $B = 3.84$ MHz.

B. Adjacent Channel Selectivity Test Case

Adjacent channel selectivity (ACS) is a measure of a receiver's ability to receive a W-CDMA signal at its assigned channel frequency in the presence of an adjacent channel signal at a given frequency offset from the center frequency of the assigned channel. ACS is the ratio of the receive filter attenuation at the assigned channel frequency to the receive filter attenuation at the adjacent channel frequencies. The ACS has to be better than 33 dB. Simultaneously, the BER shall not exceed 10^{-3} for the following test parameters (see also Fig. 3): $\hat{I}_{or}$ and DPCH_E_C are -92.7 dBm/3.84 MHz and -103 dBm/3.84 MHz, respectively. The same reference measurement channel with a symbol rate of 30 ks/s and an SG of 21 dB is used as was the case with the reference sensitivity level test case. The PSD of the adjacent channel signal ± 5 MHz away from the wanted channel is $I_{oac} = -52$ dBm/3.84 MHz. The signal levels for the ACS test case are summarized in Fig. 3.

We assume again $E_{b,\,req}/I$ to be 5 dB, IL for the baseband implementation to be 2 dB, and CG to be 4 dB, which leads to an acceptable interference level P_I of

$$P_I = \text{DPCH\_E}_C + SG + \text{CG} - \frac{E_{b,\,req}}{I} - \text{IL} = -85\ \text{dBm}. \quad (7)$$

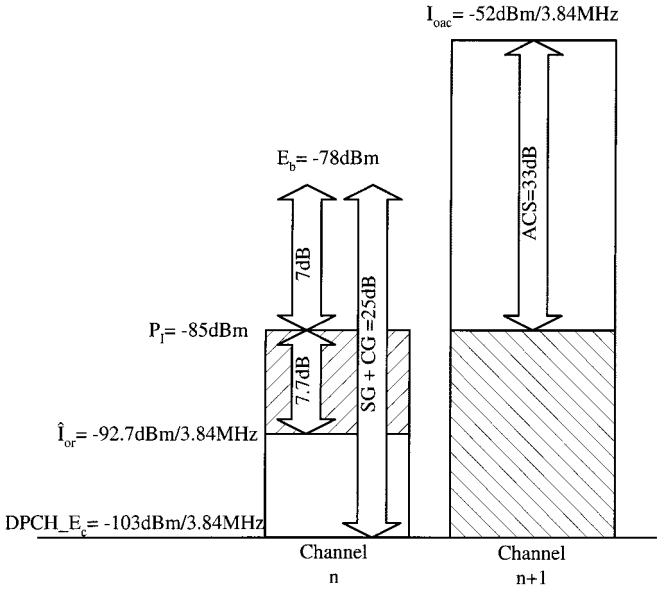

Fig. 3. Signal levels for the ACS test case.

If the adjacent channel interference signal is treated as Gaussian noise-like interference, the required ACS can be derived to be

$$\text{ACS} = I_{oac} - P_I = -52\ \text{dBm} + 85\ \text{dBm} = 33\ \text{dB}. \quad (8)$$

C. Intermodulation Test Case

For the intermodulation test case, two types of interferers are specified: a continuous wave (CW) interferer (I_{ouw1}) and a W-CDMA interference signal (I_{ouw2}). Both interferers have a power of -46 dBm, with the CW signal spaced 10 MHz away from the wanted signal and the modulated interferer having a spacing of 20 MHz. The power of the wanted channel is DPCH_$E_C = -114$ dBm/3.84 MHz and $\hat{I}_{or} = -103.7$ dBm/3.84 MHz. The modulated interference signal consists of the necessary common channels for any connection and 16 dedicated data channels with uncorrelated user data and the channelization codes for data channels are chosen to optimally reduce the peak-to-average ratio. Fig. 4 illustrates these test-case conditions. The sum of both interfering signals is transferred by means of a third-order nonlinearity into the desired channel. Therefore, this test case defines the required input intercept point of third order (IIP3) of the receiver. The acceptable noise-plus-interference level $P_{N,\,I}$ in the desired

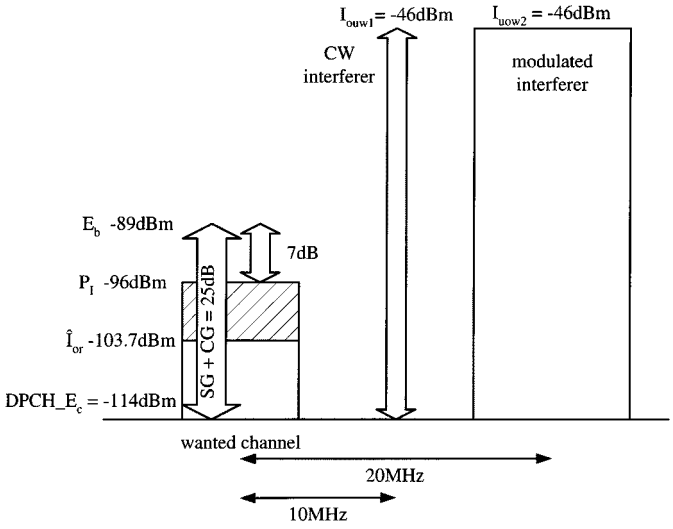

Fig. 4. Intermodulation test case.

channel must not exceed −96 dBm/3.84 MHz if we assume a combined spreading and CG of 25 dB. Before determining the required IIP3, we have to assign the total noise-plus-interference power $P_{\mathrm{N,I}}$ to their sources. According to [19], we assume the following: 50% noise power (−3 dB), 15% intermodulation power (−8 dB), 15% blocking from CW interferer (−8 dB), 15% blocking from modulated interferer (−8 dB), and 5% power from oscillator noise (−13 dB). Furthermore, we neglect second-order products. From these assumptions, we derive a tolerable level for the third-order intermodulation power of $P_{\mathrm{I,3}} = -104.2$ dBm/3.84 MHz. The required IIP3 can be derived as

$$\mathrm{IIP3} = \frac{2I_{\mathrm{ouw1}} + I_{\mathrm{ouw2}} - P_{\mathrm{I,3}}}{2} = -16.9\,\mathrm{dBm}. \qquad (9)$$

The equations used in Sections IV-A–C exemplify how the signal levels are influenced by the despreading operation and by interference sources. Further estimations like the above-mentioned ones can be found in [19]. However, one should keep in mind that these results can only serve as coarse estimates. What has been neglected in, e.g., the IIP3 calculation, is the fact that (9) is based on pure sinusoidal signals. However, the IIP3 of a nonlinear building block with respect to a W-CDMA signal is different from the IIP3 for sinusoidal signals [20]. A second point neglected in the above estimation is the fact that the modulated interference signal is a W-CDMA signal spread with other orthogonal variable spreading factor (OVSF) codes than the wanted signal. Depending on how good the orthogonality between signals that are spread with different codes is preserved [modeled by OF, see (4)], this type of interference can behave strongly different to the Gaussian noise model, which is often used for CDMA signals. These simplifications make the above computation of the required IIP3 only an estimation. Furthermore, the actual CG has to be simulated to achieve realistic values. Altogether, this leads for certain test cases to the necessity of accurate computer-aided system design using an appropriate combination of commercial baseband and microwave simulation tools like COSSAP and ADS, which, in some cases, have to be backed up with self-written user-defined codes. The maximum input level test case is such an example.

D. Maximum Input Level Test Case

The maximum input level test case defines the maximum input power at the antenna port of the mobile station at which a coded BER of at least 10^{-3} must be achieved. According to the 3GPP specifications [16], the majority of the interference consists of a signal derived from a so-called orthogonal channel noise simulator (OCNS). This signal is used to simulate other user and control signals on the orthogonal channels in the downlink. $\hat{I}_{\mathrm{or}}$ is specified to be −25 dBm/3.84 MHz with the wanted user signal level being 19 dB below. If we assume the interference coming only from the common channels and the OCNS and perform the same simplified estimations, as in the above-described test cases, we would require a combined spreading and CG of 26 dB to achieve the necessary E_{b}/I of 7 dB for a BER of 10^{-3}. However, the system simulation results displayed in Fig. 5 show different results [21]. Even an E_{b}/I of below 1.5 dB is sufficient to achieve a BER of 10^{-3}. It can be seen, that the difference between the coded and uncoded BER strongly depends on the value of E_{b}/I. The distinct BER difference between a Gaussian noise model and the OCNS interference illustrates the effect of spreading the different user signals with the theoretically orthogonal OVSF codes. It becomes clear that using filtered Gaussian noise to model the interference from other users is not valid in any case and must be considered carefully.

From the ACS test case, the required 1-dB compression point $P_{1\,\mathrm{dB}}$ of the LNA can be determined as is shown in Fig. 6.

V. Receiver Architectures

The selection of a receiver architecture is determined by several criteria like number of external components, cost, power dissipation, complexity, and, of course, the expertise and intellectual property rights of each manufacturer's RF design team. In the following, we will review the most important receiver architectures with respect to their applicability to UMTS.

A. Heterodyne Receiver

Fig. 7 shows the heterodyne receiver structure. This architecture first translates the received signal band down to some IF, which is usually much lower than the initially received frequency band. Channel selection filtering is performed at this IF frequency, which relaxes the requirements for the channel selection filter. The choice of the IF frequency incorporates a principal design tradeoff in heterodyne receiver design (see Fig. 8).

A major advantage of the heterodyne receiver structure is its adaptability to many different receiver requirements. This yields superior performance with respect to selectivity and sensitivity. Therefore, it has been the dominant choice in RF systems for many decades. However, the complexity of the structure and the need for a large number of external components (e.g., the IF filters, which in today's cellular phone systems are usually surface acoustic wave (SAW) filters [22]) make problems if a high level of integration is necessary. This is also the major drawback from the costs point-of-view. Furthermore, amplification at a high-IF frequency can cause high power consumption.

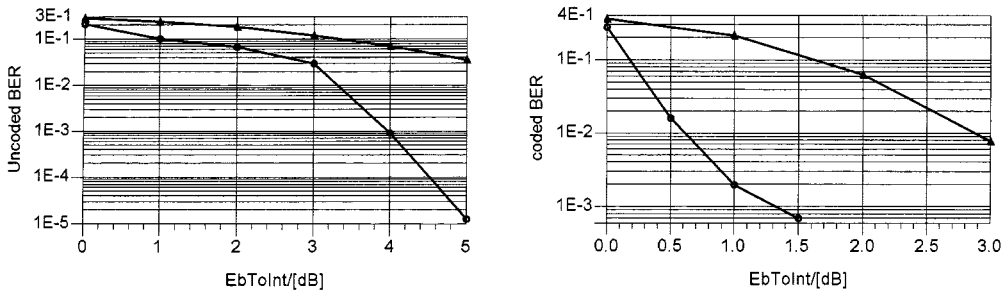

Fig. 5. Uncoded and coded BER for interference modeled as Gaussian noise (△) and OCNS signal (○).

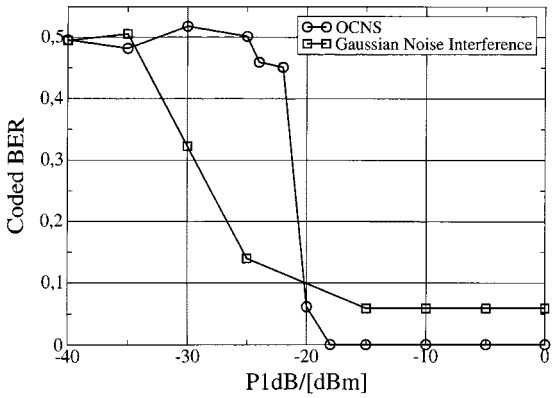

Fig. 6. Coded BER as function of the 1-dB compression point for interference modeled as OCNS signal (○) and Gaussian noise (□).

The most important disadvantage of the heterodyne receiver architecture is the missing adaptability of a single design to different wireless standards and modes. Since the external IF filter is optimized for a certain mode of operation resulting in a fixed bandwidth and center frequency, it cannot be reused for, e.g., a different mobile communication standard. Mobile terminals for UMTS will most likely be dual-mode devices supporting also a 2G standard. Such a device would need two different receive paths each with its own external IF filter, if a heterodyne structure is used. Designing heterodyne receiver architectures for multimode operation would probably result in too costly and complex solutions.

B. Homodyne Receiver

The homodyne receiver architecture (also called zero-IF or direct-conversion architecture) avoids the disadvantages of the heterodyne concept by reducing the IF to zero. This saves the (first) mixer, the (first) local oscillator (LO), and the IF channel selection filter, as can be seen from Fig. 9 and, moreover, also the image problem vanishes if a quadrature down-converter is used [23]. Thus, the simplicity of this structure offers two important advantages over its heterodyne counterpart. First the problem of image is circumvented because $f_{\mathrm{IF}} = 0$. As a result, no image filter is required. This may also simplify the LNA design because there is no need for the LNA to drive a 50-Ω load, which is often necessary when dealing with image rejection filters. Second, the IF SAW filter and subsequent down-conversion stages can be replaced by low-pass filters and baseband amplifiers that can easily be integrated. The possibility of changing the bandwidth of the integrated low-pass filters (and, thus, changing the receiver bandwidth) is a major advantage if multimode and multiband applications are of concern.

On the other hand, the zero-IF receiver topology incorporates a number of issues that do not play a role or are at least not as serious in a heterodyne receiver. Since, in a homodyne topology, the down-converted band extends to zero frequency, offset voltages can corrupt the signal and, more importantly, saturate the following stages. The following are three main ways how dc offsets can be generated:

- mixing of the LO leakage signal with the LO signal—if the LO signal leaks to the antenna, is radiated, and subsequently reflected from a moving target back to the receiver, a time varying part of the dc offset can be generated;
- self-mixing of a strong interferer due to leakage from the LNA or mixer input to the LO port;
- demodulation of a large amplitude modulated (AM) signal via second-order nonlinearity of the mixer that generates a time-varying dc offset.

The three above-described sources can easily generate a dc-offset voltage of some millivolts. Since a UMTS receiver requires about 80-dB gain, most of which is assigned to the baseband amplifiers, the analog-to-digital converter (ADC) will be driven into saturation even by such a small dc offset. In time division multiple access (TDMA) systems, idle time intervals can be used to carry out offset cancellation. This would be a practical solution for the 3GPP-TDD mode, but cannot be used for offset cancellation in the FDD mode because of the continuous signal reception. Here, the natural solution for dc-offset cancellation is high-pass filtering. Since the signal band extends from dc to approximately 2 MHz, a high-pass filter with a cutoff frequency of several kilohertz results in an acceptable degradation of the system performance [24]. This approach is only possible because of the wide-band nature of the signal. A more general dc-offset compensation approach, which is also applicable to narrow-band systems like the Japanese personal handy-phone system (PHS), is experimentally demonstrated in [25].

I/Q mismatch is another critical issue for the zero-IF receiver topology. Any mismatch distorts the constellation diagram of the baseband signal, resulting in an enhanced BER. Fortunately, pilot symbol assisted channel estimation is used in W-CDMA systems. Irrespective of the pilot symbols used (either the time multiplexed pilot symbols or the common pilot signal), this estimation can be used to compensate for I/Q phase and amplitude mismatches.

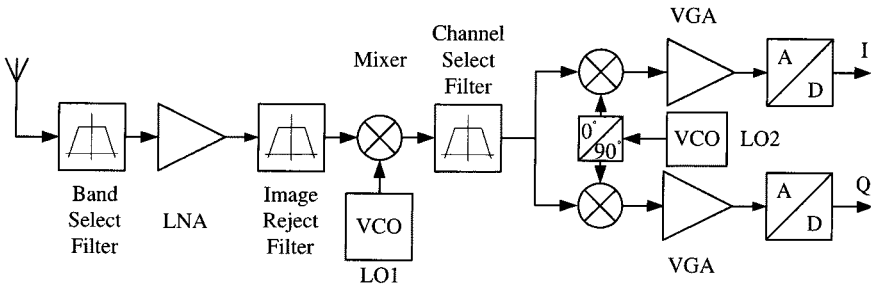

Fig. 7. Heterodyne receiver.

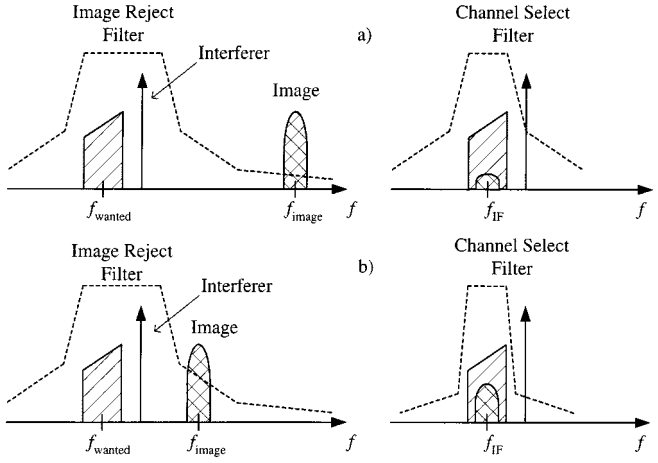

Fig. 8. Compromise selectivity for sensitivity in a heterodyne receiver. (a) High IF. (b) Low IF.

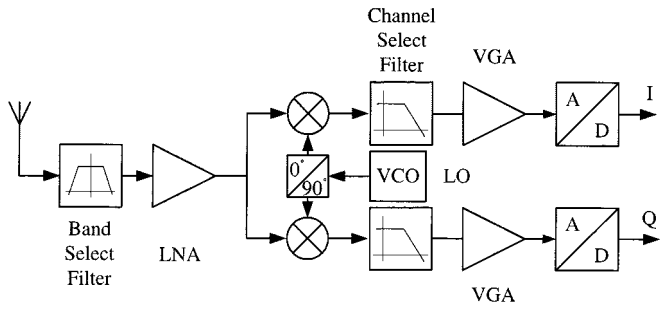

Fig. 9. Homodyne receiver.

A further severe problem associated with the homodyne receiver is flicker noise. In a wide-band system like UMTS, the impairments are lower than in narrow-band systems; however, especially for CMOS implementations, a careful design of the mixer and the following baseband circuitry is necessary for a successful implementation. Finally, LO leakage produces not only dc offsets, but also spurious emissions. In case of UMTS, these leakage must be less than -60 dBm/3.84 MHz for UE receivers.

Due to the high integration level and the possibility to electronically adapt the receiver to different bands and modes of operation, the homodyne receiver is the most promising candidate for future 3G terminals in a long-term perspective. The described problems can clearly be solved by means of improved semiconductor technology and a system-level-based optimization of the circuits and their design.

C. Wide-Band IF Receiver with Double Conversion

An alternative approach to the homodyne receiver, which is also well suited for monolithic integration, is the wide-band IF receiver with double conversion shown in Fig. 10 [26], [27]. The LNA is followed by a quadrature down-conversion to an IF. Therefore, no image problem is present in case of proper subsequent signal processing. After wide-band low-pass or bandpass filtering (depending on the chosen IF) in both branches, an image-reject structure for translating the signal to baseband follows. Using this structure, the in-phase (I) and quadrature-phase (Q) components of the wanted signal are added constructively, while the image signals are canceled. The LO for the image reject down-conversion is tunable so that the wanted channel can be properly transferred to baseband where the channel selection is performed. The idea behind this architecture is to combine the advantages of homodyne and heterodyne receivers as follows.

- The channel selection is performed in baseband, offering the possibility for multistandard operation. Since no external high-Q channel selection filters are needed, this architecture is well suited for integration.
- The LO leakage signal falls outside the receive band, thus minimizing the problem of a time varying dc offset.
- The dc offset of the first mixer stage is of no concern since it is out-of-band and can be removed by a bandpass filter. The dc offset introduced by the image-reject mixer poses only a minor problem because the signal can be amplified at the IF. Furthermore, the dc offset will be fairly constant, allowing for the efficient use of specific offset cancellation techniques.
- The first LO can be implemented at a fixed frequency with better phase-noise performance. Since the second LO operates at a much lower frequency, the phase noise performance can be far better than it is in a homodyne receiver.

The drawbacks of wide-band IF receivers are as follows.

- The second LO must be tunable over a fairly wide range of frequencies to be able to translate all possible channels down to baseband. Especially for multimode operation, this requires a broader tuning range compared to its nominal oscillation frequency than usual.
- Due to possible strong adjacent channel interference, the image reject down-converter must have a high dynamic range and linearity.
- Any I/Q mismatches limit the image reject capability and, therefore, the sensitivity of the receiver.

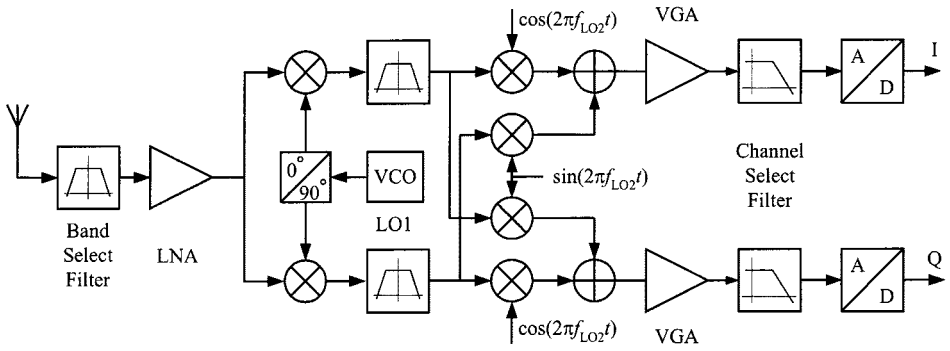

Fig. 10. Double conversion wide-band IF receiver.

The image rejection capability of the wide-band IF structure can be improved with the help of the RF front-end filter if the IF is chosen high enough. The achievable image rejection as function of the phase and gain mismatch is given by [27]

$$\text{IR [dB]} = 10\log\frac{1+(1+\Delta A)^2+2(1+\Delta A)\cos(\varphi_{\varepsilon 1}+\varphi_{\varepsilon 2})}{1+(1+\Delta A)^2-2(1+\Delta A)\cos(\varphi_{\varepsilon 1}-\varphi_{\varepsilon 2})} \quad (10)$$

where $\varphi_{\varepsilon 1}$ and $\varphi_{\varepsilon 2}$ are the deviations from quadrature in the first and second LOs, respectively, and ΔA is the accumulated gain error between the I and Q branch. To achieve more than 35 dB of image rejection, the phase error must be kept below 2° at perfect gain matching and the amplitude error must be below 3.6% at perfect phase matching. Both values are difficult to achieve in a mass-production technology. If the IF frequency is chosen high enough and an appropriate RF filter is used, a total image rejection of 60-65 dB can be expected. If we consider the out-of-band blocking test case of the UTRA FDD mode [16], a CW interferer with -30 dBm must be taken into account if the IF frequency is below 85 MHz; otherwise, the interferer can have a power of -15 dBm. The power of the wanted signal ($\mathrm{DPCH\_E_C}$) is specified to be -114 dBm/3.84 MHz and the total received PSD in the receive channel is -103.7 dBm/3.84 MHz. If we make the same assumptions as in the reference sensitivity test case (25 dB of despreading and CG), the allowed interference level is -96 dBm. The interference power level of -15 dBm is lowered to -36 dBm due to the despreading in the receiver. Therefore, an interference rejection of at least 60 dB is required.

The required dynamic range of the second mixing stage is an even more serious problem of wide-band IF receivers than the limited image rejection capability. If we consider the ACS test case, the power of the adjacent channel is specified to be about 50 dB higher than the power of the wanted user signal level ($\mathrm{DPCH\_E_C}$). The sum of both signals (and all other possible unwanted received signals) has to be processed by both mixer stages without distorting the small wanted signal. This fact and the limited image rejection capability makes the wide-band IF architecture not the first choice for an UMTS receiver.

D. Low-IF Receiver

If the IF in the receiver is low enough, it is possible to convert the IF signal to the digital domain and perform the final down-conversion in the digital signal processor (DSP) [28]–[30]. The structure is shown in Fig. 11 and is very similar to the double-conversion wide-band IF receiver. The main difference is due to the operation of the ADC at IF. This enables the image reject down-conversion to be implemented digitally and, therefore, without I/Q mismatch. A further difference to the wide-band IF architecture is due to the choice of the IF. While the IF in the latter structure is typically high, it is chosen to be as low as possible in a low-IF system to relax the requirements for the ADC. DC offsets are of no concern if bandpass filtering is applied after the first mixer stage since the digital image-reject down-conversion does not suffer from any self-mixing and leakage problems.

A disadvantage of low-IF receivers is the required high image suppression [29]. In a zero-IF receiver, the wanted signal is also the image signal, while in a low-IF receiver, the image signal can be substantially stronger than the wanted signal. For a low-IF UMTS receiver, one would choose the IF frequency at 2.5 MHz, which is the lowest possible value to minimize the ADC requirements. In this case, the adjacent channel signal is also the image signal. According to the ACS test case, this signal has about 50 dB higher power than the wanted user signal level ($\mathrm{DPCH\_E_C}$). The signal-to-interference ratio (with interference considered coming only from nonperfect image suppression) in zero-IF receivers is basically equal to the image suppression. In low-IF receivers, the achievable signal-to-interference ratio is equal to the image suppression minus the factor by which the image signal can be stronger than the wanted signal. The image suppression is determined by the matching of the first mixer stage, but can be enhanced using adaptive digital signal-processing techniques [31]. Due to the shift of the final image reject down-conversion to the digital domain, the image-reject performance of the low-IF receiver can be better than that of the wide-band IF structure. However, the high linearity requirements for the image reject down-converter in the wide-band IF receiver are shifted to the ADC in a low-IF receiver. It is necessary for the ADC to transfer all necessary information for image suppression into the digital domain. This requires the sampling of a signal composed of the wanted signal and the image signal, which can be as much as 50 dB higher. The resulting necessary high-performance ADC makes this architecture not suitable for UMTS receivers in mobile terminals with today's technology.

In [28], an analog transceiver front-end for DCS-1800 has been reported, which makes use of the low-IF architecture.

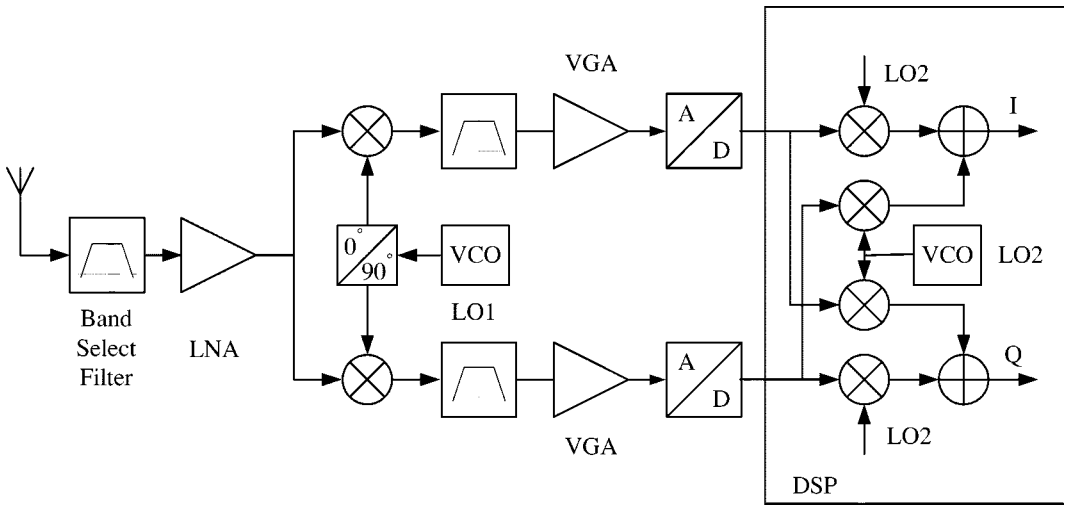

Fig. 11. Low-IF receiver.

While only the analog part is described and no specifications for the ADCs are given, the use of the low-IF concept is feasible in this case due to the chosen IF frequency of 100 kHz and the fact that the adjacent channel signal is specified to be only 9 dB above the wanted channel.

E. Digital-IF Receiver

In the heterodyne receiver architecture of Fig. 7, the second down-conversion and subsequent filtering can be performed in the digital domain. The principal issue in this approach is the performance required from the ADC. To limit the requirement on the ADC, a sufficiently low IF has to be chosen, which makes it impossible to employ bandpass filtering to suppress the image frequency. Thus, an image suppression mixer has to be used. The image suppression attainable in today's systems is limited to a range of 30–55 dB. Due to the high demands on the ADC and the image suppression mixer performance, this architecture, to the authors knowledge, up to now has only been published once for 3G terminal applications [46] (see Section VI for a description). Nevertheless, it is utilized in base stations where many channels must be received and processed simultaneously.

VI. RFICs for UMTS: Current Developments

A. Homodyne Receivers

The majority of the published work on receiver design for W-CDMA mobiles is based on the direct-conversion topology. One example of a homodyne receiver can be found in [32], [33]. Although not an integrated solution, it is described here for comparison. The whole receiver chain consists of a duplexer, LNA, RF bandpass filter, an even harmonic quadrature mixer for down-conversion [34], and an analog baseband IC [33]. The down-conversion block is realized using a completely passive even harmonic quadrature mixer composed of two antiparallel diode pairs (Fig. 12). The baseband IC [33] contains two identical I/Q receive paths to support diversity, each consisting of an LNA with 16-dB gain, a passive *RC* high pass, a fifth-order Cauer–Chebyshev low-pass filter, and a cascade of four amplifiers and three attenuators with a gain range of 95 dB in steps

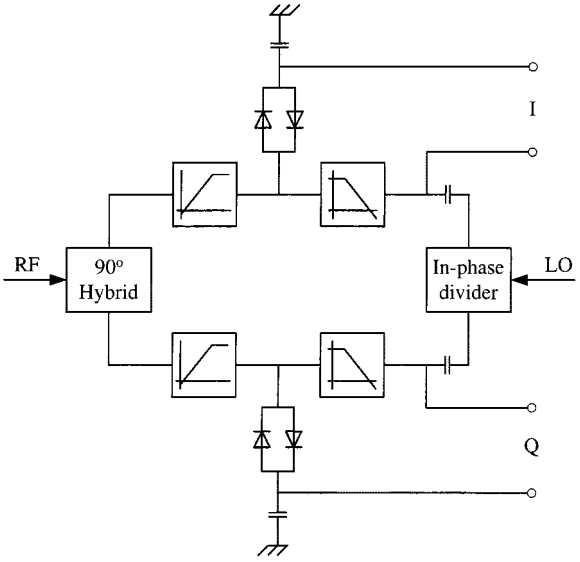

Fig. 12. Even harmonic quadrature mixer.

of 1 dB. It was fabricated with a 0.6-μm BiCMOS process and consumes 20 mA with both receive paths ON and 12 mA with only one path operating. The following performance has been measured with the whole receiver chain (duplexer, LNA, RF bandpass filter, mixer, and analog baseband IC) [32]: an NF of 5.7 dB, an IIP3 of -17.2 dBm, an IIP2 of $+26.6$ dBm, a sensitivity of -116.4 dBm, an I/Q phase mismatch of 7.7°, and an I/Q amplitude mismatch of 0.4 dB.

A second homodyne W-CDMA receiver IC described in [35] consists, besides an external RF amplifier (NF of 4 dB, 12-dB gain, IIP3 of 11 dBm), of a quadrature demodulator with an NF of 12 dB, baseband variable gain amplifiers (VGAs), and an output amplifier, which is also used as active antialiasing filter with external *R* and *C*. Between the VGA block and the output amplifier, an external *LC* low-pass filter is inserted in the signal path for channel filtering. For dc-offset cancellation, the mixer output is fed to an offset nulling circuitry via an error integrator. The corner frequency of this high pass is set to 2 kHz. The whole receiver features a gain control range of 60 dB.

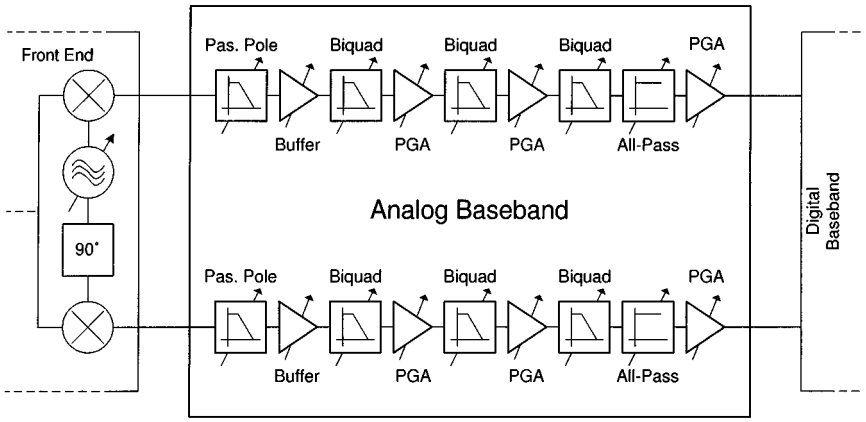

Fig. 13. Partitioning of filtering and amplification to simultaneously optimize noise and linearity.

One of the first prototype chipsets for a W-CDMA direct-conversion receiver is described in [36]. The realized receiver consists of an LNA, mixer, quadrature-phase generation network, baseband amplification and filtering, and ADCs for the I and Q path. Four different dies (RF-block, baseband-block, each ADC) have been used to avoid substrate coupling. The ADCs have been realized in 0.5-μm CMOS technology, while for the RF and baseband ICs, a 0.25-μm BiCMOS process has been used. The receiver is designed to operate in both UE and BS and the channel spacing can be selected digitally between 5–20 MHz. The LNA provides a gain of 20 dB. The on-chip second-order polyphase filter generates the needed quadrature phases from the external LO. The analog baseband processing chain includes a preamplifier, a fifth-order Butterworth active *RC* filter, output buffers, and a servo loop to filter out the dc offset in the input signal. It provides a gain range of 78 dB in 3-dB steps. The baseband filter can be programmed to 2-, 4-, and 8-MHz bandwidth to support chip-rates of 4.096, 8.192, and 16.384 Mchip/s, respectively. The filter is automatically tuned using 5-bit switched capacitor matrices and a reference time-domain test integrator. The 6-bit 16-MS/s ADCs employ a 1.5-bit/stage pipeline architecture with digital correction and interstage gain. The following performance data are given: an NF of 5.1 dB, an IIP3 of -9.6 dBm, an IIP2 of $+38$ dBm, a reference sensitivity of -114 dBm, a gain control range of 78 dB in 3-dB steps, an I/Q phase mismatch of the RFIC of below 1°, an I/Q amplitude mismatch of the RFIC of 0.6 dB, and 128-mA current consumption at 2.7-V bias voltage.

An interesting option is the use of silicon–germanium (SiGe) bipolar technology for the receiver front-end. An RFIC fabricated in SiGe technology described in [37], [38] incorporates a fully integrated voltage-controlled oscillator (VCO) together with a dual-modulus prescaler, the quadrature phase generation circuitry, the mixer, a low-noise baseband amplifier, and a low-pass blocking filter. Before entering the receiver IC, the signal is fed via a duplexer, an LNA, and an interstage SAW filter, which converts the single-ended signal into a differential one. The SAW filter also relaxes the required IIP3 and IIP2 of the following circuits since it further attenuates the transmit signal. The low-noise baseband amplifier features two gain settings and is followed by an active Butterworth-type third-order low-pass filter with a corner frequency of 5 MHz. Remarkable are the extremely low LO leakage of -95 dBm together with a high IIP2 of 55 dBm of the mixer. This results in very low dc-offset values of less than 10 mV at the baseband output of the IC. The cascaded values of IIP3 and NF are $+4$ and 15 dBm, respectively. The chip, which draws 33 mA from a 2.7-V supply, is realized in a 0.35-μm SiGe BiCMOS process with an f_T of 75 GHz.

A fully integrated analog baseband IC designed for properly interfacing the above described zero-IF receiver RFIC is demonstrated in [39]. The partitioning of filtering and amplification was chosen as to simultaneously optimize noise and linearity performance, resulting in cascading the filter blocks with programmable gain amplifiers according to Fig. 13. The circuit design of the analog baseband filter is based on extensive system simulation, as described in detail in [40], considering especially the ACS test case described above and the 3GPP blocking specifications. A thorough investigation led to the design of a seventh-order elliptic filter in combination with a third-order all-pass for phase equalization to meet the in-band distortion limits expressed by specific error vector magnitude values. The elliptic filter was realized by means of a passive pole and three elliptic biquads. The test chip is fabricated in a 0.35-μm SiGe BiCMOS technology. The total gain range is 0–55.5 dB with a resolution of 0.5 dB. The current consumption is 19.5 mA at a bias voltage of 2.7 V.

Another example for a direct-conversion receiver fabricated with a 0.35-μm 45-GHz f_{T} SiGe BiCMOS process can be found in [41]. The single-chip receiver includes an LNA, down-conversion mixers, analog channel selection filters, VGAs, and 6-bit ADCs. The performance data are an NF of 3.7 dB, an IIP3 of -16 dBm (high gain), an IIP2 of $+18$ dBm (high gain), and a 1-dB compression point of -27 dBm. The LNA features a gain of 21 dB and its output signal is ac coupled to the quadrature mixers to remove the dc component generated by the LNA nonlinearity. The channel selection is performed by a fifth-order Chebyshev-type low-pass filter and achieves an adjacent channel attenuation of 36 dB. The VGA has a gain range of 66 dB in 3-dB steps. The 6-bit ADCs use a pipeline architecture and feature a sample frequency of 15.36 MS/s. The whole IC consumes only 22 mA from a 2.7-V supply.

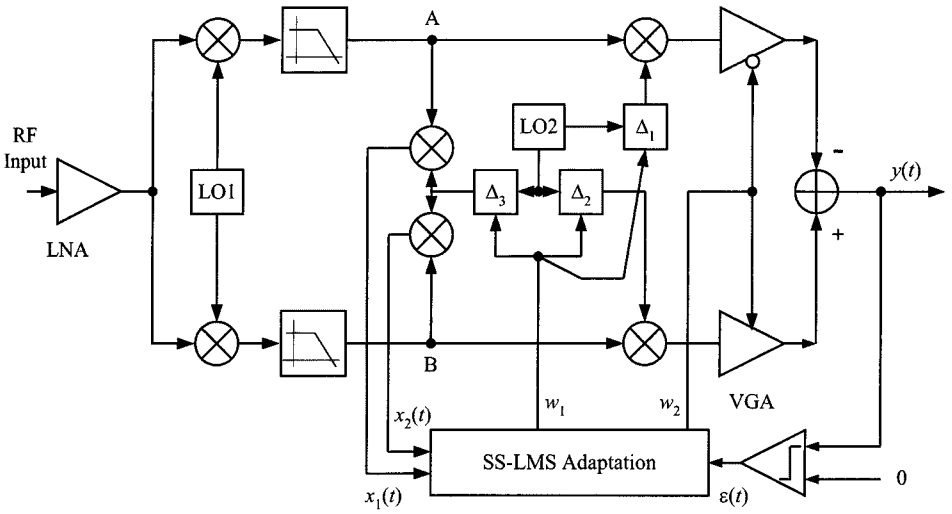

Fig. 14. CMOS Weaver-type image-reject receiver with SS-LMS calibration.

B. Heterodyne Receiver

A first UMTS IF transceiver front-end is published in [42] and [43]. Since it is based on the conventional heterodyne architecture, it features no multimode capability. The demonstrated chip-set includes two separate RFICs for transmitter and receiver, each with an on-chip synthesizer with integrated VCO tuning and tank. These IF chips were fabricated in a 0.4-μm/25-GHz silicon bipolar process, operate over a 2.7–3.3-V supply voltage and incorporate several power-down modes for a power-conscious mobile station design. The performance of receiver and transmitter comply with the Japanese Association of Radio Industry and Business (ARIB) W-CDMA and the European UMTS standard. The IF receiver IC includes two complete IF paths for antenna diversity and/or service channel monitoring and a common LO generation and distribution. Each path features a three-stage VGA with a gain range of more than 95 dB at an IF of 318 MHz, a quadrature demodulator, a fifth-order Chebyshev filter, and a first-order all-pass in front of the differential I/Q outputs. Further performance data are an NF of 5 dB, an IIP3 of -2 dBm, an I/Q phase mismatch of $\pm 2.5^{\circ}$, an I/Q amplitude mismatch of 0.8 dB, and an EVM of 6.2%. With both channels and the synthesizer in operation, the receiver consumes a maximum current of 30.2 mA at maximum gain and at 2.7-V bias voltage.

C. Other Receiver Architectures

In [44], an Weaver-type image-reject receiver fabricated in a 0.25-μm CMOS technology is described. The block diagram is shown in Fig. 14. The gain and phase mismatches, which are critical for the image rejection capability of this receiver architecture, are calibrated using a sign–sign least-mean-square (SS-LMS) algorithm. The mismatches of the second mixer stage are adjusted adaptively and differentially at the IF of 200 MHz, leaving the RF stage undisturbed. During the calibration, an image tone is applied at the RF input and the output at baseband serves as one of the three inputs for the digital SS-LMS circuit. The SS-LMS algorithm adjusts the variable delay stages (denoted by Δ) and the gain adjustment until $y(t)$ approaches zero. A prototype circuit achieved an uncalibrated image-rejection ratio (IRR) of 25 dB, which could be improved to 57 dB by means of the SS-LMS calibration. Further data are an NF of 5.2 dB, an IIP3 of -17 dBm, a voltage gain of 41 dB, and a power consumption of 55 mW during calibration and 50 mW in normal receiving mode from a 2.5-V supply.

A single-quadrature receiver architecture, which achieves a maximum IRR of 49 dB without trimming or calibration, is demonstrated in [45]. The IC, implemented in a 0.2-μm CMOS/SIMOX technology with an f_T of 40 GHz, consists of an LNA, a quadrature mixer, polyphase filters, and a buffer amplifier. The polyphase filters are used to convert the external differential LO signal into quadrature signals and to suppress the image signals at the output of the mixers. The single-ended LNA provides a gain of 12.5 dB with an NF of 3.1 dB. The phase errors in the LO signal are suppressed resulting in lower phase errors in the quadrature IF signal, which gives the high IRR of >45 dB for an IF range of 5–12 MHz. The IIP3 of the receiver is -15.7 dBm, the NF was measured to be below 10 dB, and the circuit draws 12 mA from a 1-V supply.

An integrated CMOS RF front-end for a digital IF receiver has been published in [46]. The chip consists of an LNA, a mixer, a programmable-gain amplifier (PGA), a fractional-N frequency synthesizer, and a VCO. The IF is located at 190 MHz, at which an external SAW filter removes the adjacent channels. Further external components are the RF balun, the loop filter for the RF phase-locked loop (PLL) and the decoupling capacitors. The cascaded IIP3 of LNA and mixer is -2 dBm, the double-sideband (DSB) NF and sensitivity are 3.5 dB and -108 dBm, respectively. With a PGA gain range form -40 to 40 dB switchable in 2-dB steps, the receiver features a gain range of 80 dB. The RF chip draws 52 mA from a 3-V supply.

VII. Comparison

Almost all described receiver realizations feature an IIP3 of around -16 dBm, which is sufficient to pass the intermodulation test case. Most receivers have an NF from 3.5 dB to about

6 dB. Only for the image-rejection receiver in COMS/SIMOX technology [45] values of <10 dB are reported even without any channel selection filtering. The SiGe zero-IF receiver from [41], despite including analog channel selection, features a very low NF of only 3.7 dB. However, since not all examples include the analog baseband processing, a fair comparison is difficult. This is also the case if the power dissipation is considered. With 156 mW, the power consumption of the digital IF receiver [46] even without the ADC is much higher than for all others (except for [36], which is designed for both UE and base-station use and features a much higher IIP3 of -9.5 dBm than all other implementations), which is a severe drawback for its applicability in mobile terminals. Concerning the integration, the direct-conversion architecture is most favorable. However, only the two-chip solution from [38] and [39] includes the VCO and synthesizer. The Weaver-type architecture described in [44] supports the same integration level as the direct-conversion receiver. The digital IF receiver described in [46] also includes the VCO and synthesizer, but requires an IF SAW filter.

VIII. Future Trends

A. RF CMOS Technology Approach

While CMOS technology dominates the digital domain, for a long time it was considered to not be suitable for the design of RFICs. This was due to factors like the limitation of Q values for integrated inductors to 5–10, the lack of satisfactory device models at gigahertz frequencies, or a worse g_m/I of CMOS transistors compared to bipolar transistors. Advances in CMOS technology, while mainly driven by digital needs, pushed the transit frequency of today's 0.18-μm CMOS transistors beyond 50 GHz [48]. Together with improved device modeling [47] and the growing number of interconnect layers, which allows for the realization of improved passive components, RF CMOS has become increasingly popular in the last few years. With an integral design approach, taking into account aspects from system level down to device physics, even applications in the 5-GHz range and beyond have been realized, see, e.g., [48], sometimes reusing circuit concepts from decades ago that seemed impractical for many years. Advances with respect to improved devices, circuit topologies, and system-level architecture make RF CMOS a strong contender for W-CDMA applications [49]. Probably due to the considerably higher linearity and noise requirements for 3G systems compared to WLAN systems, a fact coming from the different range and mobility scenarios for the two system types [50], only a few CMOS RFICs for 3G applications have been reported in the literature [45], [46], [44]. A further project aimed at RF CMOS design for W-CDMA transceivers is described online.[4] The results achieved thus far indicate that RF CMOS is becoming an interesting option for 3G.

B. Low-Power Design

Building wireless systems for low-power operation will probably be one of the most important design goals. This is a prerequisite for the full penetration of wireless systems in our daily life, especially for short-range communication between, e.g., cellular phones, personal digital assistants (PDAs), wrist watches, headsets, etc. Again, we have to deal with a multidisciplinary problem since transceiver architecture and circuit design determine the instantaneous power consumption, while the average power consumption depends to a large extent also on a good power management at the system and protocol levels [51], [52]. The RF power amplifier (PA) in the transmitter front-end is one of the most power-consuming building blocks in any wireless communication system. Achieving a high PA efficiency in an UMTS device is an especially challenging problem. The RF envelope shows high amplitude variations due to the linear quadrature phase-shift keying (QSPK)-like modulation scheme and the possibility of transmitting via multiple data channels [53]. This requires a linear PA operation over a wide amplitude range, which is only possible with low efficiency. However, a high PA efficiency is extremely important because the transmitter in the UMTS FDD mode is continuously active if not operated in the compressed mode [10]. Linearization techniques [54] can help to improve the PA efficiency. Also, strategies like gain switching are possible, which is also applicable for reducing the current consumption of all other amplifiers in the transceiver.

C. Integration of RF and Baseband Functionalities

The trend toward a single-chip transceiver appeared some years ago, but has meanwhile somewhat lost its attraction. Nevertheless, the steadily increasing level of integration can clearly be identified as a major future trend. This also comprises the integration of the analog front-end with the digital baseband part. There are numerous obstacles like, e.g., interference due to substrate coupling, different supply voltage requirements, heat dissipation problems, pin count, etc. However, benefits like reduced component count and required printed-circuit-board area, as well as enhanced functionality, can be attained and will fuel considerable research effort to overcome these difficulties. This trend for integration of baseband and RF sections will also take place at the system design level. The result will be the enhancement of the RF performance by means of digital signal-processing techniques such as digital predistortion for PA linearization, improved dc-offset compensation for zero-IF receivers, or the above described on-chip calibration of an image-reject receiver [44].

D. Software-Defined Radio

The concept of software radio [55] is an emerging technology enabling the development of flexible multistandard/multiservice radio systems, reconfigurable and adaptable by software. Initially the ideal software-radio concepts refers to an architecture with the entire signal processing performed in the digital domain, analog-to-digital (ADC) and digital-to-analog (DAC) conversion assumed outright at the antenna. For wireless communication systems at 2 GHz and above, this seems not to be realizable in the near future. However, recent advances in digital transceiver design, incorporating digital down-converters and digital up-converters in combination with suitable ADCs and DACs shift the digital signal-processing edge to IF frequencies [56]. Nevertheless, there will always remain some essential RF

[4][Online]. Available: http://www.iis.ee.ethz.ch/nwp/lemon/lemon.html

signal processing like antialiasing filtering and flexible (i.e., not only switchable) multiband and multimode RF front-end functionalities. An example for the latter issue is described in [57], where a flexible front-end is demonstrated for operation in the frequency band from 800 to 2200 MHz with variable channel bandwidths of up to 5 MHz, as is required for UMTS. The circumvention of tight RF band filtering as applied in current single-band designs is fundamental to reach this target. A successful application of wide-band RF filtering, covering all frequency bands of interest, combined with a subsequent high-IF stage and active interference cancellation is demonstrated. The high-IF frequency following the RF stage allows image (respectively sideband) rejection. Direct feedthrough of the TX signal into the RX path is greatly suppressed by this new active cancellation technique.

IX. Conclusion

The paper has presented a review of cellular phone receiver concepts for IMT-2000 system use. It has been shown how basic equations lead to an estimation of the transceiver system requirements. Examples have exhibited the influence of 3GPP test cases on key parameters for the receiver design. Furthermore, the most popular receiver architectures have been investigated. Their suitability for W-CDMA systems has been evaluated and possible problems have been addressed. Recent work on receiver RFICs for use in W-CDMA mobiles including direct-conversion, heterodyne, digital IF, and image-reject architectures have been presented. Finally, some possible future trends in W-CDMA transceiver design have been addressed. In particular, the development of RF CMOS technologies and software radio-like front-end concepts should be investigated carefully to evaluate more accurately their potential for future applications.

Acknowledgment

The authors wish to thank all their colleagues at the University of Linz, Linz, Austria, Danube Integrated Circuit Engineering (DICE), Linz, Austria, and Infineon Technologies, Munich, Germany, who contributed to this paper.

References

[1] A. Mehrotra, *GSM System Engineering*. Norwood, MA: Artech House, 1997.
[2] J. C. Haartsen, "The Bluetooth radio system," *IEEE Pers. Commun.*, vol. 7, pp. 28–36, Feb. 2000.
[3] R. van Nee, G. Awater, M. Morikura, H. Takanashi, M. Webster, and K. W. Halford, "New high-rate wireless LAN standards," *IEEE Commun. Mag.*, vol. 37, Dec. 1999.
[4] H. Sari, "A state-of-the-art-review of broadband wireless access," in *Proc. Eur. Wireless Technol. Conf.*, Paris, France, Oct. 2000, pp. 310–315.
[5] T. Ojanperä and R. Prasad, Eds., *Wideband CDMA for Third Generation Mobile Communications*. Norwood, MA: Artech House, 1998.
[6] P. Taaghol, B. G. Evans, E. Buracchini, R. De Gaudenzi, G. Gallinaro, J. H. Lee, and C. G. Kang, "Satellite UMTS/IMT-2000 W-CDMA air interfaces," *IEEE Commun. Mag.*, vol. 37, pp. 116–126, Sept. 1999.
[7] J. Cai and D. J. Goodman, "General packet radio service in GSM," *IEEE Commun. Mag.*, vol. 35, pp. 122–131, Oct. 1997.
[8] P. Chaudhury, W. Mohr, and S. Onoe, "The 3GPP Proposal for IMT-2000," *IEEE Commun. Mag.*, vol. 37, pp. 72–81, Dec. 1999.
[9] "IMT-2000 radio interface specifications approved in ITU meeting in Helsinki," ITU, Press Release ITU/99-22, Nov. 1999.
[10] H. Holma and A. Toskala, Eds., *WCDMA for UMTS*. New York: Wiley, 2000.
[11] C. E. Shannon, "A mathematical theory of communication," *Bell Syst. Tech. J.*, vol. 27, pp. 379–423, 623–656, July 1948.
[12] R. C. Dixon, *Spread Spectrum Systems With Commercial Applications*, 3rd ed. New York: Wiley, 1994.
[13] S. Glisic and B. Vucetic, *Spread Spectrum CDMA Systems for Wireless Communications*. Norwood, MA: Artech House, 1997.
[14] G. L. Stüber, *Principles of Mobile Communication*. Norwell, MA: Kluwer, 1994.
[15] M. K. Simon, J. K. Omura, R. A. Scholtz, and B. K. Levitt, *Spread Spectrum Communications Handbook*, rev. ed. New York: McGraw-Hill, 1994.
[16] "UE Radio transmission and reception (FDD)," Tech. Specification Group, 3GPP, (TSG) RAN WG4, TS 25.101 v4.0.0, Mar. 2001.
[17] "Terminal conformance specification: Radio ception (FDD)," Tech. Specification Group, 3GPP, (TSG) TS 34.121 v3.5.0, June 2001.
[18] "MS receiver sensitivity in UTRA FDD mode," TSG-RAN Working Group 4, Nokia, Doc. TSGW4 #1(99)005, Jan. 1999.
[19] O. K. Jensen, T. E. Kolding, C. R. Iversen, S. Laursen, R. V. Reynisson, J. H. Mikkelsen, E. Pedersen, M. B. Jenner, and T. Larsen, "RF receiver requirements for 3G W-CDMA mobile equipment," *Microwave J.*, vol. 43, no. 2, pp. 22–46, Feb. 2000.
[20] H. Pretl, L. Maurer, W. Schelmbauer, R. Weigel, B. Adler, and J. Fenk, "Linearity considerations of W-CDMA frontends for UMTS," in *Proc. IEEE MTT-S Microwave Symp. Dig.*, Boston, MA, July 2000, pp. 433–436.
[21] L. Maurer, W. Schelmbauer, H. Pretl, A. Springer, B. Adler, Z. Boos, and R. Weigel, "Influence of receiver frontend nonlinearities on W-CDMA signals," in *Proc. Asia–Pacific Microwave Conf.*, Sydney, NSW, Australia, Dec. 2000, pp. 249–252.
[22] L. Maurer, W. Schelmbauer, H. Pretl, Z. Boos, R. Weigel, and A. Springer, "Impact of IF-SAW filtering on the performance of a W-CDMA receiver," in *Proc. IEEE Int. Ultrason. Symp. Dig.*, San Juan, Puerto Rico, Oct. 2000, pp. 375–378.
[23] B. Razavi, *RF Microelectronics*. Engelwood Cliffs, NJ: Prentice-Hall, 1999.
[24] J. H. Mikkelsen, T. E. Kolding, T. Larsen, T. Klingenbrunn, K. I. Pedersen, and P. Mogensen, "Feasibility study of DC offset filtering for UTRA-FDD/WCDMA direct-conversion receiver," in *Proc. 17th IEEE NORCHIP Conf.*, Oslo, Norway, Nov. 1999, pp. 34–39.
[25] H. Tsurumi, M. Soeya, H. Yoshida, T. Yamaji, H. Tanimoto, and Y. Suzuki, "System-level compensation approach to overcome signal saturation, DC offset, and 2nd-order nonlinear distortion in linear direct conversion receiver," *IEICE Trans. Electron.*, vol. E82-C, no. 5, pp. 708–716, May 1999.
[26] S. Mirabbasi and K. Martin, "Classical and modern receiver architectures," *IEEE Commun. Mag.*, vol. 38, pp. 132–139, Nov. 2000.
[27] J. C. Rudell, J.-J. Ou, T. B. Cho, G. Chien, F. Brianti, J. A. Weldon, and P. R. Gray, "A 1.9-GHz wide-band IF double conversion CMOS receiver for cordless telephone applications," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2071–2088, Dec. 1997.
[28] M. S. J. Steyaert, J. Janssens, B. De Muer, M. Borremans, and N. Itoh, "A 2-V CMOS cellular transceiver front-end," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1895–1907, Dec. 2000.
[29] J. Crols and M. S. J. Steyaert, "Low-IF topologies for high-performance analog front ends of fully integrated receivers," *IEEE Trans. Circuits Syst. II*, vol. 45, pp. 269–282, Mar. 1998.
[30] ——, "A single-chip 900 MHz CMOS receiver front-end with a high-performance low-IF topology," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1483–1492, Dec. 1995.
[31] L. Yu and W. M. Snelgrove, "A novel adaptive mismatch cancellation system for quadrature IF radio receivers," *IEEE Trans. Circuits Syst. II*, vol. 46, pp. 789–801, June 1999.
[32] K. Itoh, T. Katsura, H. Nagano, T. Yamaguchi, Y. Hamade, M. Shimozawa, N. Suematsu, R. Hayashi, W. Palmer, and M. Goldfarb, "2 GHz band even harmonic type direct conversion receiver with ABB-IC for W-CDMA mobile terminal," in *Proc. IEEE MTT-S Int. Microwave Symp. Dig.*, Boston, MA, June 2000, pp. 1957–1960.
[33] M. Goldfarb, W. Palmer, T. Murphy, R. Clarke, B. Gilbert, K. Itoh, T. Katsura, R. Hayashi, and H. Nagano, "Analog baseband IC for use in direct conversion W-CDMA receivers," in *Proc. IEEE RFIC Symp. Dig.*, Boston, MA, June 2000, pp. 79–82.
[34] M. Shimozawa, T. Katsura, N. Suematsu, K. Itho, Y. Isota, and O. Ishida, "A passive-type even harmonic quadrature mixer using simple filter configuration for direct conversion receiver," in *Proc. IEEE MTT-S Int. Microwave Symp. Dig.*, Boston, USA, June 2000, pp. 517–520.

[35] B. Sam, "Direct conversion receiver for wide-band CDMA," in *Proc. Wireless Symp.*, 2000, pp. SAM-1–SAM-5.
[36] A. Pärssinen, J. Jussila, J. Ryynänen, L. Sumanen, and K. A. I. Halonen, "A 2-GHz wide-band direct conversion receiver for WCDMA applications," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1893–1903, Dec. 1999.
[37] H. Pretl, W. Schelmbauer, B. Adler, L. Maurer, J. Fenk, and R. Weigel, "A SiGe-bipolar down-conversion mixer for a UMTS zero-IF receiver," in *Proc. IEEE Bipolar/BiCMOS Technol. Meeting*, Minneapolis, MN, Sept. 2000, pp. 40–43.
[38] H. Pretl, W. Schelmbauer, L. Maurer, H. Westermayr, R. Weigel, B.-U. Klepser, B. Adler, and J. Fenk, "A W-CDMA zero-IF front-end for UMTS in a 75 GHz SiGe BiCMOS technology," in *Proc. IEEE RFIC Symp.*, Phoenix, AZ, May 2001, pp. 9–12.
[39] W. Schelmbauer, H. Pretl, L. Maurer, R. Weigel, B. Adler, and J. Fenk, "A fully integrated analog baseband IC for an UMTS zero-IF receiver," in *Proc. AustroChip 2000*, Graz, Austria, pp. 8–15.
[40] L. Maurer, W. Schelmbauer, H. Pretl, B. Adler, A. Springer, and R. Weigel, "On the design of a continuous-time channel select filter for a zero-IF UMTS receiver," in *Proc. IEEE 51st Veh. Technol. Conf.*, Tokyo, Japan, May 2000, pp. 650–654.
[41] J. Jussila, R. Ryynänen, K. Kivekäs, L. Sumanen, A. Pärssinen, and K. Halonen, "A 22 mA 3.7 dB NF direct conversion receiver for 3G WCDMA," in *IEEE Int. Solid-State Circuits Conf. Dig.*, Feb. 2001, pp. 284–285.
[42] W. Thomann, J. Fenk, R. Hagelauer, and R. Weigel, "Fully integrated W-CDMA IF receiver and transmitter including IF synthesizer and on-chip VCO for UMTS mobiles," in *Proc. IEEE Bipolar/BiCMOS Technol. Meeting*, Minneapolis, MN, Sept. 2000, pp. 36–39.
[43] W. Thomann, J. Fenk, R. Hagelauer, and R. Weigel, "Fully integrated W-CDMA IF receiver and transmitter including IF synthesizer and on-chip VCO for UMTS mobiles," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1407–1419, Sept. 2001.
[44] L. Der and B. Razavi, "A 2 GHz CMOS image-reject receiver with sign-sign LMS calibration," in *IEEE Int. Solid-State Circuits Conf. Dig.*, Feb. 2001, pp. 288–2895.
[45] M. Ugajin, J. Kodate, and T. Tsukahara, "A 1 V 12 mW receiver with 49 dB image rejection in CMOS/SIMOX," in *Solid-State Circuits Conf. Dig.*, Feb. 2001, pp. 294–295.
[46] K. Lim, C.-H. Park, H. K. Ahn, J. J. Kim, and B. Lim, "A fully integrated CMOS RF front-end with on-chip VCO for WCDMA applications," in *2001 IEEE Int. Solid-State Circuits Conf. Dig.*, Feb. 2001, pp. 286–287.
[47] B. Razavi, "CMOS technology characterization for analog and RF design," *IEEE J. Solid State Circuits*, vol. 34, pp. 268–276, Mar. 1999.
[48] T. H. Lee and S. S. Wong, "CMOS RF integrated circuits at 5 GHz and beyond," *Proc. IEEE*, vol. 88, pp. 1560–1571, Oct. 2000.
[49] J. H. Mikkelsen, T. E. Kolding, and T. Larsen, "RF CMOS circuits target IMT-2000 applications," *Microwaves RF*, pp. 99–107, July 1998.
[50] P. G. Baltus and R. Dekker, "Optimizing RF front ends for low power," *Proc. IEEE*, vol. 88, pp. 1546–1559, Oct. 2000.
[51] A. A. Abidi, G. J. Pottie, and W. J. Kaiser, "Power-conscious design of wireless circuits and systems," *Proc. IEEE*, vol. 88, pp. 1528–1545, Oct. 2000.
[52] B. A. Meyers, J. B. Willingham, P. Landy, M. A. Webster, P. Frogge, and M. Fischer, "Design considerations for minimal-power wireless spread spectrum circuits and systems," *Proc. IEEE*, vol. 88, pp. 1598–1612, Oct. 2000.
[53] A. Springer, T. Frauscher, B. Adler, D. Pimingsdorfer, and R. Weigel, "Impact of nonlinear amplifiers on the UMTS system," in *Proc. IEEE Sixth Int. Spread Spectrum Commun. Symp.*, Parsippany, NJ, Sept. 2000, pp. 465–469.
[54] P. B. Kenington, *High-Linearity RF Amplifier Design*. Norwood, MA: Artech House, 2000.
[55] W. H. W. Tuttlebee, "Software-defined radio: Facets of a developing technology," *IEEE Pers. Commun.*, vol. 6, pp. 38–44, Apr. 1999.
[56] D. Efstathiou and Z. Zvonar, "Enabling components for multi-standard software radio base stations," *Wireless Pers. Commun.*, vol. 13, no. 1, pp. 145–166, 2000.
[57] W. Schacherbauer, A. Springer, T. Ostertag, C. C. W. Ruppel, and R. Weigel, "A flexible multiband frontend for software radios using high IF and active interference cancellation," in *Proc. IEEE MTT-S Int. Microwave Symp. Dig.*, Phoenix, AZ, May 20–25, 2001, pp. 1085–1088.

Andreas Springer (S'90–A'97–M'99) was born in Linz, Austria, in 1966. He received the Dipl.-Ing. degree in electrical engineering from the Technical University of Vienna, Vienna, Austria, in 1991, and the Dr.Techn. (Ph.D.) degree and Univ.-Doz. (habilitation) degree from the University of Linz, Linz, Austria, in 1996 and 2001, respectively.

From 1991 to 1996, he was with the Microelectronics Institute, University of Linz. Since 1997, he has been an Assistant Professor at the Institute for Communications and Information Engineering, University of Linz. He has been engaged in research on GaAs integrated millimeter-wave transferred electron devices (TEDs), monolithic microwave integrated circuits (MMICs), and millimeter-wave sensor systems. His current research interests are focused on simulation of wireless communication systems, spread-spectrum communications, linearization of PAs, direct conversion architectures, UMTS, orthogonal frequency division multiplexing (OFDM), and RFICs. In these fields, he has authored or co–authored over 70 papers in journals and international conferences.

Dr. Springer is a member of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S), the IEEE Communications Society, and the IEEE Vehicular Technology Society.

Linus Maurer was born in Steyr, Austria, in 1972. He received the Dipl.-Ing. degree in physics and the Ph.D. degree from the University of Linz, Linz, Austria, in 1997 and 2001, respectively.

Since 1998, he has been with the Institute of Communications and Information Engineering, University of Linz. Since January 2000, he has been engaged in an European Commission (EC) co-founded project, which deals with the development of an RF-CMOS based UMTS compliant transceiver front end, as Technical Leader for the system simulation portion. His main research interest covers the field of system simulation, taking into account RF-related nonidealities. He is also interested in the simulation of mixed-signal systems. He has authored and co-authored publications in the field of wireless system design and has given international presentation and tutorials on 3G system issues.

Robert Weigel (S'88–M'89–SM'95) was born in Ebermannstadt, Germany, in 1956. He received the Dr.-Ing. and Dr.-Ing.habil. degrees in electrical engineering and computer science from the Munich University of Technology, Munich, Germany, in 1989 and 1992, respectively.

From 1982 to 1988, he was a Research Engineer at the Munich University of Technology. From 1988 to 1994, he was a Senior Research Engineer at the Munich University of Technology. From 1994 to 1996, he was a Professor of RF circuits and systems at the Munich University of Technology. In winter 1994–1995, he was a Guest Professor of SAW technology at the Vienna University of Technology, Vienna, Austria. Since 1996, he has been Director of the Institute for Communications and Information Engineering, University of Linz, Linz, Austria. In August 1999, he co-founded the Danube Integrated Circuit Engineering (DICE), Linz, Austria, which is now an Infineon Technologies Development Center devoted to the design of mobile radio circuits and systems. In 2000, he became a Professor of RF engineering at Tongji University, Shanghai, China. He has been engaged in research and development on microwave theory and techniques, integrated optics, high-temperature superconductivity, SAW technology, and digital and microwave communication systems. In these fields, he has authored or co-authored over 200 papers and has given over 120 international presentations. His review work includes European research projects and international journals.

Dr. Weigel is a member of the Institute for Components and Systems of The Electromagnetics Academy, the German Informationstechnische Gesellschaft (ITG), and the Australian Engineering Society (ÖVE). Within the IEEE Microwave Theory and Techniques Society (IEEE MTT-S), he is the chair of the Austrian IEEE COM/MTT-S joint chapter, Region 8 coordinator, regional distinguished microwave lecturer, and chair of MTT-2 microwave acoustics.